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A Flux Controlled Memristor using 90nm Technology

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***Abstract**: A flux-controlled memristor using complementary metal–oxide–(CMOS) structure is presented in this study. The proposed circuit provides higher power efficiency, less static power dissipation, lesser area, and can also reduce the power supply by using CMOS 90nm technology. The circuit is implemented based on the use of a second-generation current conveyor circuit (CCII) and operational transconductance amplifier (OTA) with few passive elements. The proposed circuit uses a current-mode approach which improves the high-frequency performance. The reduction of a power supply is a crucial aspect to decrease the power consumption in VLSI. An offered emulator in this proposed circuit is made to operate incremental and decremental configurations well up to 26.3 MHZ in cadence virtuoso platform gpdk using 90nm CMOS technology. proposed memristor circuit has very little static power dissipation when operating with ±1V supply. Transient analysis, memductance analysis, and dc analysis simulations are verified practically with the Experimental demonstration by using ideal memristor made up of ICs AD844AN and CA3080, using multisim which exhibits theoretical simulation are verified and discussed.*

***Index Terms**: current mode, memristor, emulator, pinched hysteresis loop, current conveyor (CCII), operational transconductance amplifier (OTA).*

I. INTRODUCTION

The fabrication of memristors Tio_2 material has caught attention worldwide was developed by HP laboratories in 2008 [1] due to unique behavior and characteristics. In this Tio_2 model, crossbar architecture is used which acts as a switch. Chua [2] proposed the fundamental fourth nonlinear circuit as memristor using the symmetry equations governing the fundamental passive circuit theory shown in Fig(a). Memristor is a contraction of memory resistor which exactly it functions that is it remembers its history. Memristor defines as a semiconductor that varies resistance as a function of flux (Φ) and charge (q) shown in fig(b). when power off it remembers its past resistance values. Chua [3] postulated and derived the general properties of memristive system. however, it is not experimentally done. The Tio_2 model in 2008 is the only missing link between flux and charge fabricated by a nanoscale device is costly.

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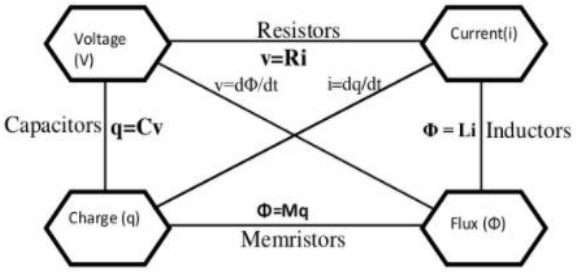

Fig(a)

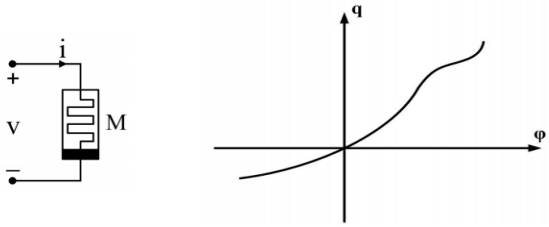

Fig (b)

Fig (1): fig(a) Symmetry relationships of Chua fig (b) ideal memristor symbol and graph

An ideal memristor must follow three characteristics[4].1)the pinched hysteresis should be in a voltage-current plane when driven by a bipolar periodic signal.2)the lobe area of the hysteresis loop should increase monotonically when excitation frequency decreases and vice versa.3) pinched hysteresis loop shrinks to a single-valued function when the frequency approaches infinite. that is, it acts as a linear resistor with high frequency.

An emulator circuit that mimics the memristor characteristics.it also exhibits non-volatility, that is, memristance of the emulator remains unchanged when no input signal is applied. the direction of the charge flow defines the memristance of the circuit, whereas the charge flowing through the memristor determines the resistance. In the absence of the electric charge, the final value of the resistance is retained which makes memristor act like a nonlinear resistor with memory. This nonvolatile property provides memristors to act as a memory. The compatibility of a memristor with CMOS technology [5] has gained momentum that many researchers to explore its application further. Memristor operates in an incremental mode of operation when memristance increases due to the flow of electric charge along the bar direction of memristor, whereas it operates in the decremental mode of configuration when its

memristance decreases due to the flow of electric charge along the direction opposite to the bar of the memristor. The memristors certainly have potential applications such as chaotic circuits [6]– [9], digital logic neuromorphic systems [10], signal processing [11], programmable analog circuits [12], oscillators [13], and have numerous other prospects.

Literature survey reveals several SPICE macro models are presented. However, SPICE macro models can only characterize static behavior instead of the dynamic behavior of a memristor [14] and real-world applications cannot be obtained using these models. A memristor emulator uses an IC AD844AN and an analog multiplier has been represented in [15], but active and passive components required for implementing the emulator circuit are more. In [16], a memristor emulator in an incremental configuration using four CCIIs and one multiplier with few passive components. In [17], one DDCC and multiplier as one active element have been used to design a memristor emulator, where the circuit performs well up to 1 MHz A floating memristor [18] has been presented using CCTA as an active element along with some passive components. Two CFOAs as an active element and one diode as a nonlinear element have been presented in [19] to implement an emulator circuit effectively. A flux-controlled floating-type memristor emulator has been used in [20] using two OTAs and one capacitor which can operate well up to 8 MHz in [21], one CCTA and one CCII as an active element have been used to implement the grounded-type memristor emulator which can work well up to 5 MHz.

In this paper, the implementation and simulation of a flux-controlled memristor using 90nm technology are presented. It is based on a flux-controlled memristor emulator using 180nm technology [22]. The proposed CMOS-based, flux-controlled memristor emulator which exhibits the characteristics possessed by an HP Tio_2 model has been presented using one CCII and OTA each as an active element. OTA at input terminal connections can be interchanged to operate the incremental and decremental modes of emulator circuit.

In section II, the proposed current conveyor and OTA USING 90nm technology is discussed. Section III shows a design of the flux-controlled memristor. Section IV discusses the ideal memristor using multisim. Section V shows the simulation and experimental results of circuits. Conclusions and summary are given in section VI.

II. DESIGN OF BUILDING BLOCKS OF MEMRISTOR

The current conveyor (cc)was introduced in 1968 by Adel sedra opening the way to current mode techniques. over the past decades, there have been numerous types of CC.one of them is CCII. It can be considered as the basic current-mode building block because all other active devices can be made up of a suitable connection of one or two CCIIs. The current conveyors are unity-gain active elements that exhibit high linearity, high-frequency performance, and a wide dynamic range than their voltage-mode counterparts. A CCII is a three-terminal active element whose port relationship is given as shown.

$$IY = 0, I Z = I X, V X = VY.$$

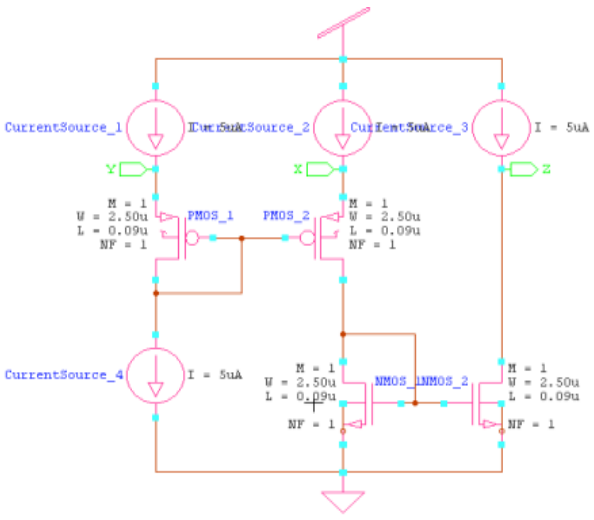

Fig 2. CMOS implementation of CCII

Port Y of the CCII is used as a voltage input and port Z is used as a current output port. Whereas, port X can be used as a current input port or as a voltage output port. Therefore, this current conveyor can be used to process both current and voltage signals. This CCII is having only four transistors comparing to an existing one.

The OTA is a transconductance device so that the differential input voltage controls the output current employing device transconductance (gm) the equation is as shown. That's why OTA is called a voltage-controlled current source

$g_m = k/\sqrt{2}\,(V_B - Vss - 2Vth)$, $I_O = g_m\,(V_P - V_N)$.

Where k is a parameter that depends on oxide thickness, width &length of the MOS parameter.

$$k = \mu_N C_{OX} W / L,$$

Transistors	W/L in µm
M_1-M_4	17/0.35
M_5-M_7	12/0.05
M_8-M_{11}	14/0.05

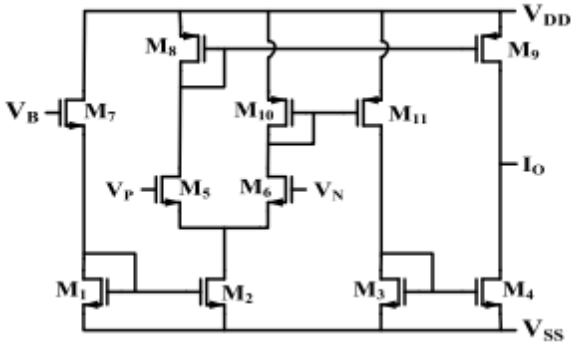

Fig.3. Operational transconductance amplifier (OTA) and transistor values.

III. PROPOSED FLUX CONTROLLED MEMRISTOR

A flux-controlled, CMOS-based memristor emulator circuit design comprising of both CCII and OTA as active elements each with a resistor and capacitor as passive elements has been used.

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The OTA at the input terminal connections is interchanged to operate the emulator. The frequency and amplitude of the input signal can be varied to get the memductance characteristics. The presented circuit works in the decremental configuration when the switch S is connected to A, whereas the other terminal is grounded and works in the incremental configuration when the switch S is connected to B.Considering the ideal behavior of the memristor emulator circuit, the analysis produces the voltage at terminals Yand X of CCII and is equal to the applied input voltage (Vin). The current flowing through the X and Z terminals of CCII is the same and is given as

$$I_X = I_Z = Vin/\ R. \qquad (1)$$

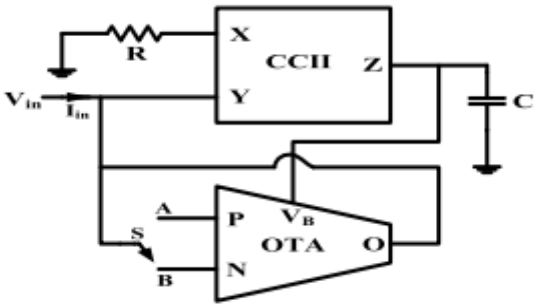

Fig.4. memristor block diagram.

The potential developed at the Z terminal of CCII can be written as

$$V_Z = 1\ /C \int Vin/\ R\ dt. \qquad (2)$$

The Z terminal of a CCII is shorted to biasing voltage V_B of the OTA. The potential is at the terminals can be written as shown.

$$V_Z = V_B = \varphi_{in}/\ RC. \qquad (3)$$

The circuit will work in the decremental configuration when the switch S is connected to A and Bis grounded. The potential at the N terminal of the OTA is the same as the applied input voltage (Vin) when the switch S is connected to B. The current flowing through the output terminal of the OTA is opposite in polarity but same as that of the input current given as

$$I_O = -I_{in}. \qquad (4)$$

The input current can be obtained by putting the value of V_B in transconductance (gm) equation (2) and can be rewritten as

$$I_{in} = \frac{k}{\sqrt{2}}\ [\varphi_{in}/RC - VSS - 2Vth]\ Vin. \qquad (5)$$

Hence, the memductance of the proposed grounded flux controlled memristor emulator in the incremental configuration is obtained as

$$W(\varphi_m) = Iin\ /Vin = -\frac{k}{\sqrt{2}}(VSS + 2Vth) + \frac{k}{\sqrt{2}}\varphi_{in}\ RC. \qquad (6)$$

Similarly, with the change in connection from the switch S to B and A grounded, the incremental configuration of the emulator circuit can be achieved. It can be observed from (6) that memductance of the emulator circuit can be controlled by applying a current or voltage signal across the memristor. Moreover, it depends on the flux, so it is defined as flux controlled memristor emulator. The memductance equation (6) consists of a linear time-varying resistor and a time-varying resistor. The presented flux-controlled memristor emulator is grounded type. In this proposed memristor we overcome the problems of the higher area in the current conveyor compared to the existing memristor and reduced the power supply from 1.5 v to 1v that leads to less static power dissipation.

IV. IDEAL MEMRISTOR USING MULTISIM

The ideal flux-controlled memristor emulator circuit utilizing the current-mode approach was built on the multisim using available ICs CA3080 and AD844AN with some passive resistors and capacitors to verify the working of the emulator circuit. Through passive elements. The gain of the OTA can be adjusted. Furthermore, the proposed memristor emulator is suitable for both breadboard and CMOS implementations. A sinusoidal voltage signal is applied at the input of the emulator circuit to get a frequency-dependent pinched hysteresis loop, which is the fingerprint of a memristor. The values for the resistor and voltage supply respectively chosen as 40K and ±10V, and the capacitor value varies with operating frequency in the voltage-current plane using the oscilloscope in multisim.

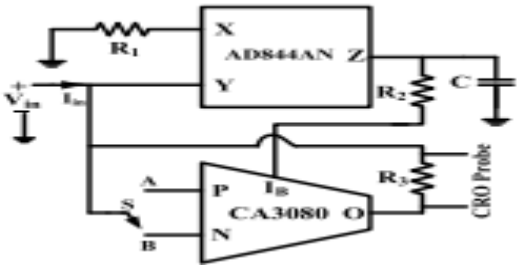

Fig.5. Ideal memristor block diagram.

The experiment has been performed at frequencies 500 and 1000 kHz, and 1, 1.4, and1.8 MHz the distortions have been found in the hysteresis loop when the frequency is increased further due to the frequency limitations of the ICs. It can be observed that the hysteresis loop becomes deformed, resulting in an asymmetrical behavior due to the errors tracking, mismatch, and parasitic components in the transistors. The loop becomes a single valued function or narrower when the frequency is increased. The prototype circuit made on a multisim or a breadboard has frequency limitations and it can be noted that the operating bandwidth of the experimental setup is around 2 MHz since these ICs have parasitic effect and frequency limitations due to interconnection. The slight deviation in the desired output can be minimized by using the offset elimination method [26] or operating biased transistors. It can be observed that the pinched hysteresis loop depends on the operating frequency and behaves like a linear resistor.

VI. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed flux-controlled memristor circuit has been simulated in the Cadence Virtuoso design tool using a 90nm GPDK process parameter under the supply voltage of ±1V to verify its response with the theoretical analysis used the multisim. The CMOS-based structure of the analog building blocks OTA and CCII has been presented in Section II.

The transistors used for CMOS implementation of the active element must be operated in the saturation region only. The memristive characteristics have been verified by applying a 1V sinusoidal input signal to the presented emulator circuit and the pinched hysteresis loop for different frequencies can be observed. In order to show memristor characteristics, the values of the passive components are C which varies from 160 to 0.5 pF and R=40K are chosen to work at a frequency range up to 25 MHz It can be observed from all the simulated results that the to hold the hysteresis loop at a higher frequency Capacitor value has been reduced. It can be observed that the area of the pinched hysteresis loop decreases with increasing frequency.

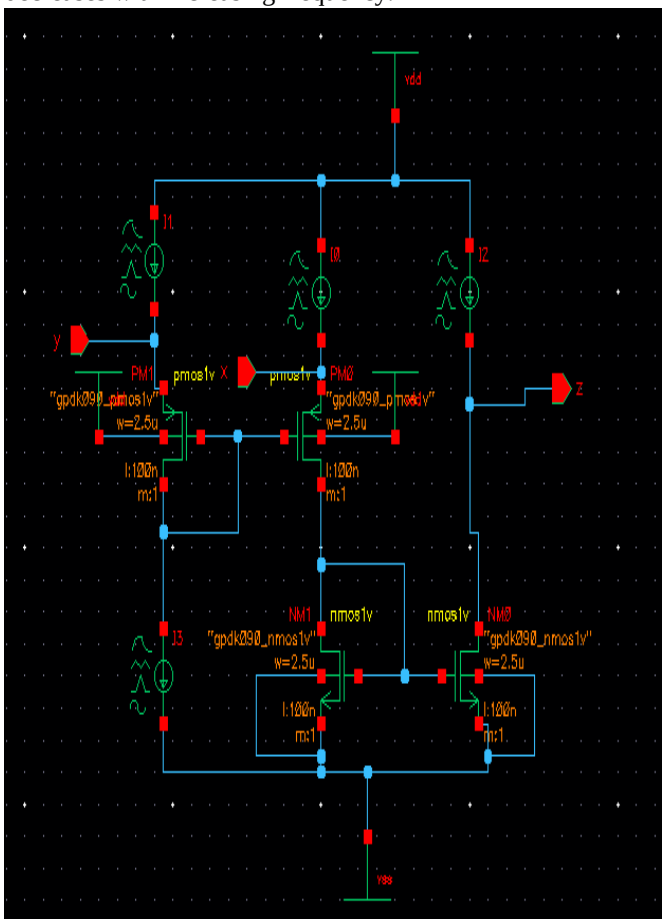

Fig.6. Simulated circuit of a current conveyor (CCII) (fig 2).

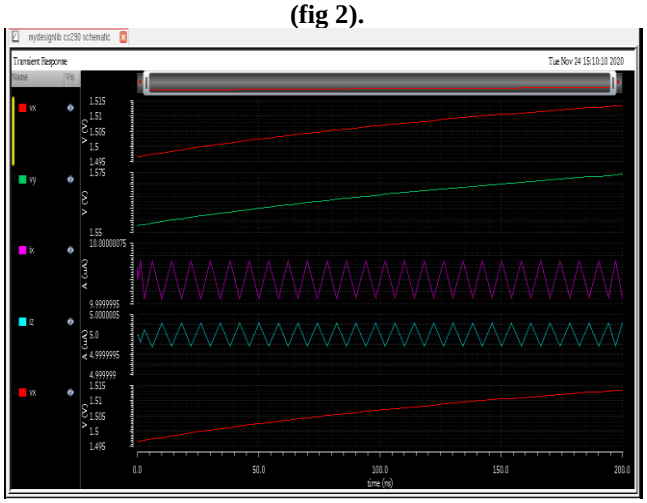

Fig. 7. Simulation waveforms of CCII (fig.2)

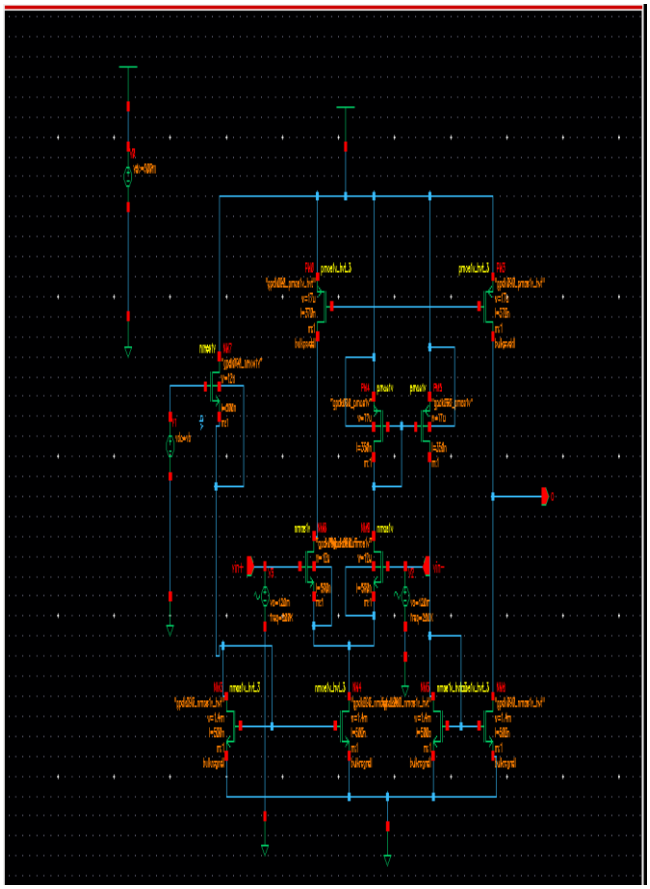

Fig.8. Simulated circuit of OTA for fig (3).

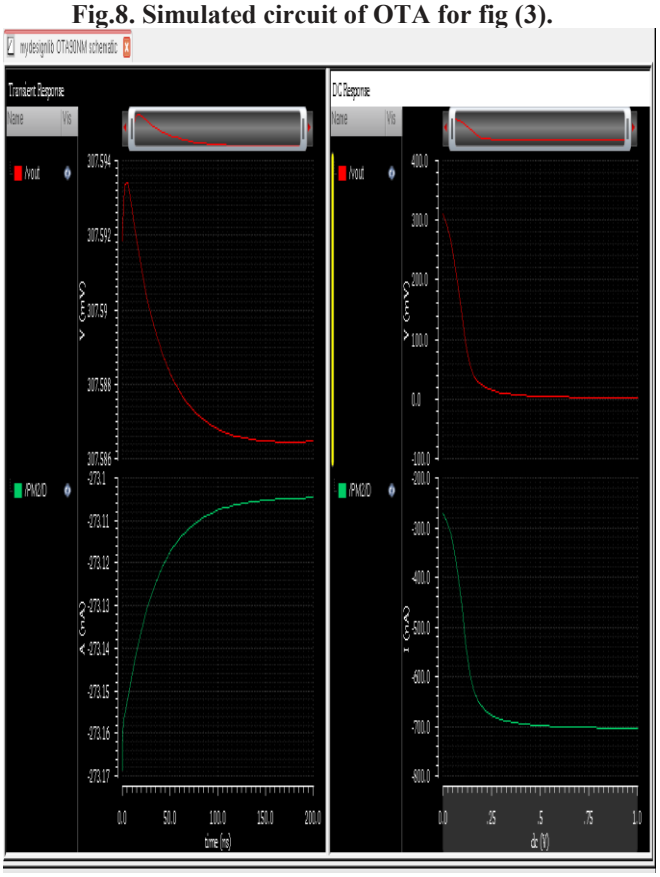

Fig.9. Simulated waveforms of OTA for fig (3).

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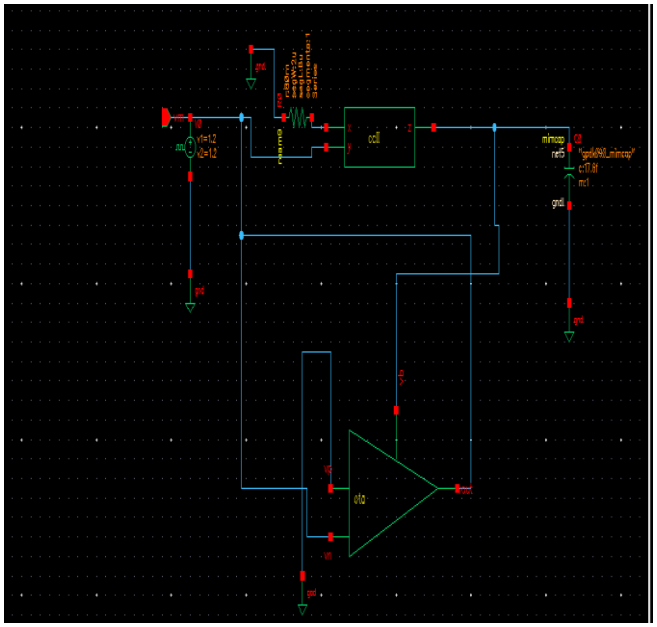

Fig.10. simulated circuit of the memristor.

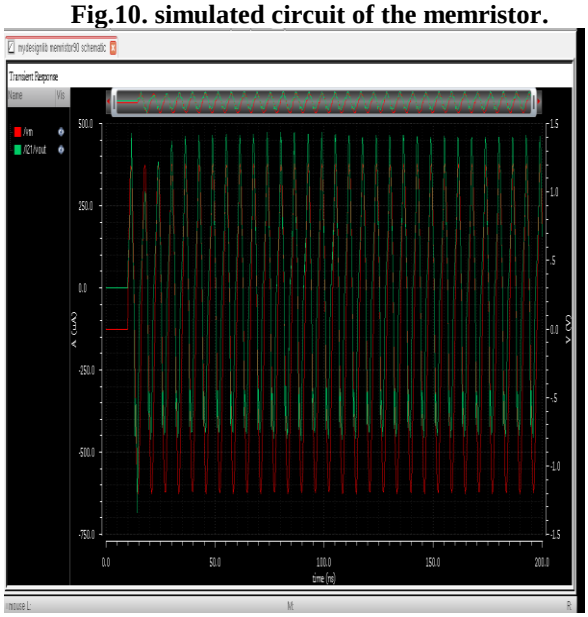

Fig .11. transient analysis of memristor at 1.2V.

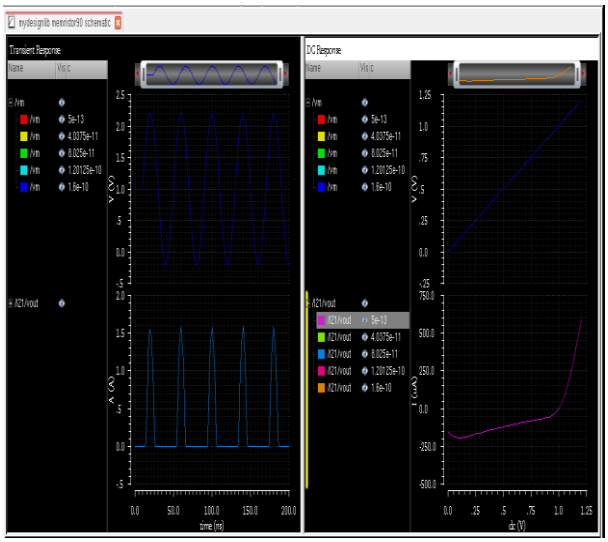

Fig. 12. Transient &dc analysis (pinched hysteresis loop) of memristor at 1V.

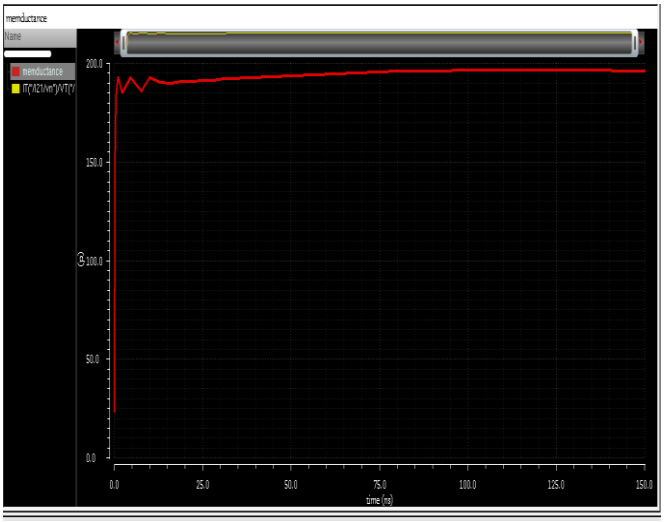

Fig.13. incremental analysis of memristor emulator.

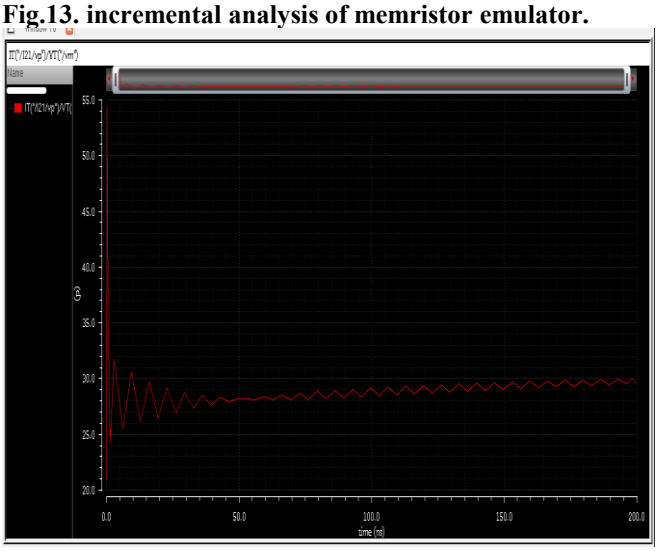

Fig.14. decremental analysis of memristor emulator

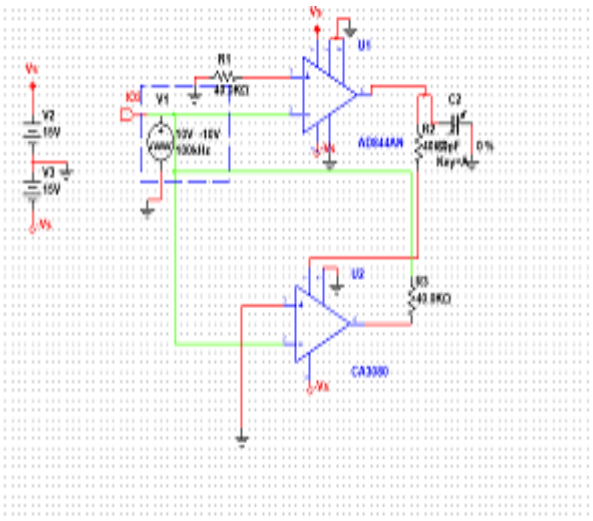

Fig.15.Simulation diagram of ideal memristor using multisim.

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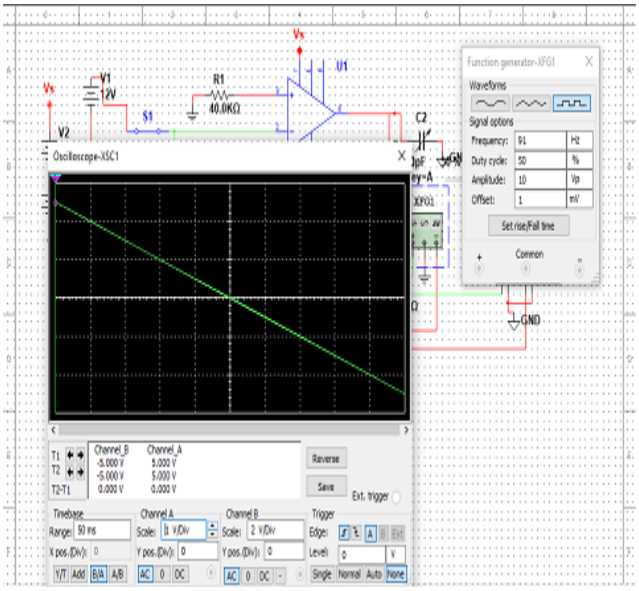

Fig.16. pinched hysteresis of an ideal amplifier.

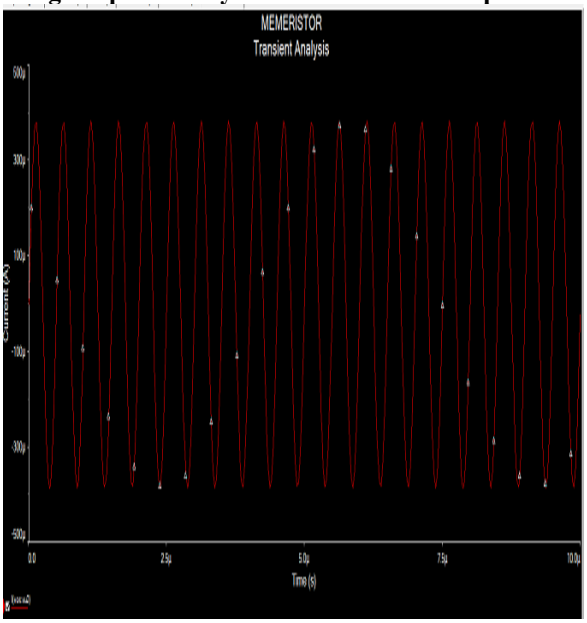

Fig.17. transient analysis of ideal memristor.

VII. CONCLUSION

Analysis of CMOS-based flux controlled memristor emulator are presented. The proposed memristor compared to the existing memristor reduced the area, power supply, and channel length. That causes less static power dissipation the performance of the circuits is validated through cadence virtuoso simulation using 90-nm CMOS technology.

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